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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorn y Dock t No. 040373/0300

Applicant: Toshiyuki HIROTA et al.

Title: SEMICONDUCTOR DEVICE WITH HIGH- AND LOW-DENSITY REGIONS OF TRANSISTOR ELEMENTS ON SINGLE SEMICONDUCTOR SUBSTRATE, AND METHOD OF MANUFACTURING SUCH SEMICONDUCTOR DEVICE

Serial No.: 09/741,195

Filed: December 21, 2000

Examiner: Vu, Quang D.

Art Unit: 2811

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §1.56 and 37 CFR §1.97

Commissioner for Patents
Washington, D.C. 20231

Sir:

Submitted herewith on Form PTO-SB/08 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR 1.56. A copy of each listed document is being submitted to comply with the provisions of 37 CFR 1.97 and 1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a prima facie prior art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The instant Information Disclosure Statement is being filed before the mailing date of the final action under 37 C.F.R. §1.113. Accordingly, pursuant to 37 C.F.R. §1.97(c), a certification or fee is required. Applicant is providing a certification below in lieu of the fee.

CERTIFICATION

The undersigned hereby certifies in accordance with 37 C.F.R. §1.97(e)(1) that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to the filing of this Statement.

RELEVANCE OF EACH DOCUMENT

A translation of a portion of a Japanese Office Action that issued September 11, 2002 with respect to a counterpart Japanese patent application is provided below.

> "The inventions as per the following claims of this application could have been easily invented based on the inventions described in the publications indicated below, which had been distributed in Japan or abroad prior to the filing of this application, by a person having ordinary knowledge in the technical field of the invention prior to the filing of this application, and therefore cannot be patented, as per the stipulations of Article 29, Section 2 of the Patent Law.
>
> Description (See the List of Cited Literature for a list of the cited literature.)

Claims 1 through 10
Reason A
Cited Literature 1 through 7

Remarks

Cited Literature 1 describes, in a manufacturing method for semiconductor integrated circuits having a high-density region and a low-density region, heat treating in a pyro (water vapor) atmosphere and reflowing the interlayer insulating film when embedding an interlayer insulating film in areas having concavities and convexities. (See in particular paragraph {0019}, paragraph {0020}, Figure 13 and the descriptions of the drawings.)

Cited Literature 2 describes, in a method for manufacturing circuits having a memory cell part with MOS transistors integrated at high density and a peripheral circuit part with MOS transistors integrated at low density, forming a nitride film over the gates, forming an interlayer insulating film over said nitride film, and reflowing the interlayer insulating film. (See in particular paragraphs {0100} to {0107}, Figure 27 and the descriptions of the drawings.)

Cited Literature 3 describes making the insulating film around gate electrodes of MOS transistors of memory cells and peripheral circuits a nitride film. (See in particular paragraph {0034}, Figure 3 and the descriptions of the drawings.)

Cited Literature 4 describes masking only the memory cell part, etching the nitride film of the peripheral circuit part, and exposing the gate oxide film in the gaps between gate electrodes. (See in particular paragraphs {0027} to {0043}, Figure 1, Figure 3 and the descriptions of the drawings.)

Regarding performing hydrogen sintering (hydrogenation processing) to recover the interface state of MOS transistors, see Cited Literature 5 (in particular, paragraph {0019}) and Cited Literature 6 (in particular, paragraph {0097}).

Furthermore, Cited Literature 7 describes exposing the semiconductor substrate surface in the gaps between gate electrodes of MOS transistors of peripheral circuits and then forming a nitride film on said semiconductor substrate surface. (See in particular Figure 4 and the descriptions of the drawings.)

List of Cited Literature

1. Japanese Unexamined Patent Application Publication H06-244383
2. Japanese Unexamined Patent Application Publication H09-219517
3. Japanese Unexamined Patent Application Publication H09-298283
4. Japanese Unexamined Patent Application Publication H11-087653
5. Japanese Unexamined Patent Application Publication H05-160362
6. Japanese Unexamined Patent Application Publication H06-268177
7. Japanese Unexamined Patent Application Publication H09-116113

Record of Prior Art Literature Search Results

Fields searched - IPC 7th Edition - H01L 27/108
H01L 21/8242

Prior art literature

Japanese Unexamined Patent Application Publication H07-086426

This Record of Prior Art Literature Search Results does not constitute a reason for rejection."

Applicant's statements regarding the Japanese Office Action are based on a partial translation that Applicant's representative obtained. These statements should in no way be considered as an agreement by Applicant with, or an admission of, what is asserted in the Japanese Office Action.

Applicant respectfully requests that the listed documents be considered by the Examiner and formally be made of record in the present application and that an initialed copy of Form PTO SB/08 be returned in accordance with MPEP §609.

Respectfully submitted,

October 23, 2002
Date

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